

| University of Mumbai                        |                       |               |       |
|---|-----------------------|---------------|-------|
| CLASS: T.E. (Electronics Engineering)       |                       | Semester - VI |       |
| SUBJECT: Computer Organization (Elective-1) |                       |               |       |
| Periods per week<br>(Each of 60 min.)       | Lecture               | 4             |       |
|   | Practical             | 2             |       |
|   | Tutorial              | -             |       |
|   |                       | Hours         | Marks |
| Evaluation System                           | Theory Examination    | 3             | 100   |
|   | Practical examination | -             | -     |
|   | Oral Examination      | 3             |       |
|   | Term Work             | -             | 25    |
|   | Total                 |               | 125   |

### Objective:

The subject of Computer Organization shall lay a strong fundamental base in understanding the functional and design aspects of various units of digital computer. The emphasis shall be on understanding of Hardware issues in computer design while addressing a number of software issues related to instruction execution, storage allocation etc.

### Prerequisite:

Fundamentals of Microprocessor Architecture, Memory interfacing

| Module | Contents  | Hours |
|--------|---|-------|
| 1      | <b>Basic Processing Unit –</b> <ul style="list-style-type: none"> <li>• CPU Organization</li> <li>• Some Fundamentals like register transfer, fetching and storing a word from memory</li> <li>• Execution of an Instruction including branch</li> <li>• The data path design</li> </ul> Fixed Point Arithmetic- Addition, Fast Addition, Multiplication, Division Algorithms   | 8     |
| 2      | <b>Control Unit –</b> <ul style="list-style-type: none"> <li>• Hardwired Control: Design Example of Multiplier / Divisor</li> <li>• Micro programmed Control: Design Examples</li> <li>• Performance Enhancement using Pipelining: Introduction, Data Hazards, Instruction hazards, Super scalar Architecture</li> </ul>  | 8     |
| 3      | <b>Memory Organization –</b> <ul style="list-style-type: none"> <li>• Memory System: Multiple Level Memories, Concept of cache and Virtual Memory, Address translation, segmentation, paging, TLB, Memory Allocation, Replacement policies</li> <li>• Cache System:               <ul style="list-style-type: none"> <li>-Cache architectures: Look through and Look Aside</li> <li>-Cache organizations: direct and associative mapping</li> <li>- Replacement Algorithms, Hit Ratio, performance of cache memory</li> </ul> </li> </ul> | 8     |

|   |   |   |
|---|---|---|
| 4 | <b>Input / Output Organization –</b><br>-I/O devices types and access methods,<br>-Interrupts and DMA,<br>-Types of busses and bus arbitration, Synchronous and Asynchronous Bus<br>-I/O interface – serial and parallel ports<br>-Storage Devices – Organization, Access techniques of magnetic hard disks and optical disks | 8 |
| 5 | <b>Introduction to Intel IA32 architecture</b><br>- Intel IA32 architecture: pipelined<br>- Register Structure, Addressing Modes<br>- Advancements in arithmetic and Logical instructions<br>- Exception handling in IA32 architecture  | 8 |
| 6 | <b>Introduction to ARM</b><br>- The ARM Family architecture (RISC)<br>- Register Structure<br>- Memory Access and addressing modes<br>- Arithmetic and Logical Instructions<br>- Branching Instructions   | 8 |

### Suggested Books:

1. Hamacher, Vranesic, Zaky: Computer Organization, Tata McGraw hill, Fifth Edition
2. John P Hayes: Computer Architecture and Organization, Tata McGraw hill
3. Hennessy and Patterson: Computer Organization and Design , Morgan Kauffman

### Practical list

1. Writing program and Simulation of Arithmetic algorithms (2)  
(Like Booth Multiplier / Division Algorithm etc)
2. Writing program and Simulation for Control Unit (1)  
(Like ALU design)
3. Writing program to evaluate various replacement policies (1)
4. Simple programs using Arithmetic and Logical instructions of IA32 Processor (2)  
(Like ASCII to BCD Conversion, multiplication etc)
5. Assignment on I/O organization (1)
6. Program / Assignment on ARM processor (2)
7. Assignment on Cache Memory Design (1)

**Term work:**

Term work shall consist of minimum eight experiments and two assignments and term work test.

The distribution of marks for term work shall be as follows:

Laboratory work (Experiments and Journal) : 10 marks.

Test (at least one) : 10 marks.

Attendance : 05 marks.

The final certification and acceptance of term-work ensures the satisfactory performance of laboratory work and minimum passing in the term-work.

**Theory Examination:**

1. Question paper will comprise of total 7 questions, each of 20 marks.
2. Only 5 questions need to be solved.
4. Question number 1 will be compulsory and will cover all modules.
5. Remaining questions will be from the same module or mixed in nature. (e.g.- suppose Q.2 has part (a) from, module 3 then part (b) will be from any module other than module 3.)
6. In the question paper, weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
7. No question should be asked from pre-requisite module